In the Claims:

1. (Currently Amended) A method of data retrieval comprising the steps of:

providing a first memory circuit;

providing a stride prediction table (SPT) that is indexed with cache line miss information;

providing cache memory circuit;

executing instructions for accessing data within the first memory;

detecting a cache miss; [[and]]

only allowing accesses[[ing]] to the SPT in response to the detection of a cache miss; and

~~updating~~ only allowing updates to the SPT ~~only when~~ in response to the detection of a cache miss ~~is detected~~.

2. (Original) A method according to claim 1 wherein the cache memory circuit is a stream buffer.

3. (Original) A method according to claim 1 wherein the cache memory circuit is a random access cache memory.

4. (Original) A method according to claim 1 wherein the cache memory circuit and the SPT are within a same physical memory space.

5. (Original) A method according to claim 1 wherein the first memory is an external memory circuit separate from a processor executing the instructions.

6. (Original) A method according to claim 1 wherein the step of detecting a cache miss includes the steps of determining whether an instruction being executed by the processor is a memory access instruction, when the instruction is a memory access instruction, determining whether data at a memory location of the memory access instruction is

present within the cache; and when the data is other than present within the cache, detecting a cache miss.

7. (Original) A method according to claim 1 wherein the step of detecting a cache miss includes the steps of determining whether an instruction to be executed by the processor is a memory access instruction; when the instruction is a memory access instruction, determining whether data at a memory location of the memory access instruction is present within the cache; and, when the data is other than present within the cache, detecting a cache miss, and accessing and updating the SPT only when the cache miss has occurred.

8. (Currently Amended) A method according to claim 1, wherein the step of allowing access[[ing]] provides a step of filtering that prevents unnecessary access and updates to entries within the SPT.

9. (Original) A method according to claim 1, wherein the cache memory circuit is integral with the processor executing the instructions.

10. (Previously presented) A method according to claim 1, wherein the SPT comprises an address field, and where a size of the address field is less than an address space used to index the SPT.

11. (Currently Amended) An apparatus comprising: a stride prediction table (SPT) that is indexed with cache line miss information; and, a filter circuit for use with the SPT, the filter circuit ~~for determining instances wherein~~ preventing both accesses and updates to the SPT ~~is to be accessed and updated, the instances only occurring when~~ unless a cache miss is detected.

12. (Original) An apparatus according to claim 11 comprising a memory circuit, the memory circuit for storing the SPT therein.

13. (Original) An apparatus according to claim 12 comprising a cache memory, the cache memory residing within the memory circuit.

14. (Original) An apparatus according to claim 13, wherein the memory circuit is a single ported memory circuit.

15. (Currently Amended) An apparatus according to claim 13, wherein the memory circuit is a random access memory circuit.

16. (Currently Amended) An apparatus ~~method~~ according to claim 11, wherein the cache memory circuit is a stream buffer.

17. (New) A method of data retrieval comprising the steps of:

providing a first memory circuit;

providing a stride prediction table (SPT) that is indexed with cache line miss information;

providing cache memory circuit;

executing instructions for accessing data within the first memory;

detecting a cache miss; and

restricting accesses to the SPT in response to the detection of a cache miss.

18. (New) A method according to claim 17, wherein the step of restricting provides a step of filtering that prevents unnecessary access and updates to entries within the SPT.

19. (New) A method according to claim 17, wherein the cache memory circuit is integral with the processor executing the instructions.

20. (New) A method according to claim 17, wherein the SPT comprises an address field, and where a size of the address field is less than an address space used to index the SPT.